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EXAMINER	
SCHILLINGER, LAURA M	
ART UNIT	**PAPER NUMBER**
2813	

NOTIFICATION DATE	DELIVERY MODE
07/27/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/668,186	TAKAFUJI ET AL.	
	Examiner	Art Unit	
	Laura M. Schillinger	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16 and 18-58* is/are pending in the application.

4a) Of the above claim(s) *1-15 and 39-57* is/are withdrawn from consideration.

5)☐ Claim(s) *28 and 37* is/are allowed.

6)☐ Claim(s) *16,18-21,23-27,29-36 and 38* is/are rejected.

7)☐ Claim(s) *22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 16, 18-21, 23-24, 29-34, and 58 are rejected under 35 U.S.C. 102(b) as being anticipated by Yudasaka (JP 06-011729).

16. A semiconductor device, comprising:

a non-single-crystal silicon thin-film device manufactured from a non-single-crystal silicon thin film (204) and a single-crystal silicon thin-film device manufactured from a single-crystal silicon thin film (203/202), wherein the non-single-crystal silicon thin-film device and the single-crystal silicon thin-film device are provided in different areas of an insulating substrate (201) (Abs.see all- Representative Drawing 2) wherein a nearest surface of the non-single-crystal silicon thin-film and a nearest surface of the single-crystal silicon thin-film are at different heights above the insulating substrate(Abs- teaching that the single crystal layers are thicker than the polysilicon structure- therefore they would be higher than the polysilicon layer 204).

18. The semiconductor device as defined in claim 16, wherein, each of the non-single-crystal silicon thin-film device and the single-crystal silicon thin-film device either a MOS thin-film transistor or a MIS thin-film transistor (Abs- TFT is understood to be a MISFET).

19 . The semiconductor device as defined in claim 18, wherein, in the MOS thin-film transistor, a gate, a gate insulating film, and silicon are formed on the insulating substrate in this order (0020).

20. The semiconductor device as defined in claim 18, wherein, a thickness of a silicon thin film of the MOS thin-film transistor is about not more than 600 nm (0017).

21. The semiconductor device as defined in claim 18, wherein, a thickness of a single-crystal silicon thin film of the MOS thin-film transistor is about not more than 100 nm (0017) .

23. The semiconductor device as defined in claim wherein, the non-single-crystal silicon thin-film device is either a MOS non-single-crystal silicon thin-film transistor or a MIS non-single-crystal silicon thin-film transistor, and the single-crystal silicon thin-film device is a bipolar single-crystal silicon thin-film transistor (Fig.4).

24. The semiconductor device as defined in claim 17, wherein, the non-single-crystal silicon thin-film device is either a MOS non-single-crystal silicon thin-film transistor or a MIS non-single-crystal silicon thin-film transistor, and the single-crystal silicon thin-film device includes

at least either one of a MOS single-crystal silicon thin-film transistor and a bipolar single-crystal silicon thin-film transistor (Fig.4).

29. The semiconductor device as defined in claim 23, wherein, a thickness of the single-crystal silicon thin film of the bipolar single-crystal silicon thin-film transistor is about not more than 800 nm (0017).

30. The semiconductor device as defined in claim 16, wherein, the non-single-crystal polycrystalline silicon thin film or a continuous grain silicon thin film, and a MOS thin-film transistor manufactured from the non-single-crystal silicon thin film includes a non-single-crystal silicon, a gate insulating film, and a gate on the insulating substrate in this order (Fig.4).

31. The semiconductor device as defined in claim 16, wherein, the non-single-crystal silicon thin film is either one of a polycrystalline silicon thin film or a continuous grain silicon thin film, and a MOS thin-film transistor manufactured from the non-single-crystal silicon thin film includes a gate, a gate insulating film, and a non-single-crystal silicon on the insulating substrate in this order (0017-0021).

32. The semiconductor device as defined in claim 16, wherein, the non-single-crystal silicon thin film is an amorphous silicon thin film, and a MOS thin-film transistor or a MIS thin-film transistor, which is manufactured from the non-single-crystal silicon thin film, includes a gate, a gate insulating film, and a non-single-crystal silicon on the insulating substrate in this order (0017-0021).

33. The semiconductor device as defined in claim 16, silicon thin film is either a wherein, the non-single-crystal silicon . thin film is an amorphous silicon thin film, and a MOS thin-film transistor or a MIS thin-film transistor, which is manufactured from the non-single-crystal silicon thin film, includes a non-single-crystal silicon, a gate insulating film, and a gate on the insulating substrate in this order (0017-0021).

34. The semiconductor device as defined in claim 16, wherein, a difference of linear expansion between a single-crystal silicon constituting the single-crystal silicon thin-film device and the insulating substrate is about not more than 25Oppm, within a temperature range from a substantially room temperature to 600 (inherent property of the materials disclosed for a silicon single crystal layer and the insulated substrate).

58. The semiconductor device as defined in claim 16, wherein the single crystal thin film is bonded with the insulating thin-film device with the insulating substrate via an intervening inorganic insulating film (0013).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yudasaka as applied to claim 16 above, and further in view of Spitzer et al (WO/93/15589).

Yudasaka teaches forming a MOSFET however fails to teach the following claimed limitations.

Spitzer teaches the following claimed limitations as cited below:

25. The semiconductor device as defined in claim 17, wherein, the non-single-crystal silicon thin-film device is either a MOS non-single-crystal silicon thin-film transistor or a MIS non-single-crystal silicon thin-film transistor, and the single-crystal silicon thin-film device includes a MOS single-crystal silicon thin-film transistor, and an image sensor including a Schottky or PN-junction diode or a CCD image sensor (page 52, lines: 1-20).

26. The semiconductor device as defined in claim 24, wherein, a thickness of a single-crystal silicon thin-film of the MOS single-crystal silicon thin-film transistor is thinner than a thickness of a single-crystal silicon thin film of the bipolar single-crystal silicon thin-film transistor (page 28, lines: 1-5 and page 18, line: 25).

27. The semiconductor device as defined in claim 23, wherein, the bipolar single-crystal silicon thin-film transistor has such a structure that a base area, a collector area, and an emitter area are formed and provided in one plane (Fig.25B and page 52, lines: 1-20).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to further include the circuitry as recited in claims 25-27 because such circuitry is considered to be conventional in the art of microdevices and the inclusion of additional circuitry is often necessary to form functional devices.

Claims 35-36 rejected under 35 U.S.C. 103(a) as being unpatentable over Yudasaka as applied to claim 16 above, and further in view of Okabe et al ('099).

Yudasaka teaches the limitations of claim 16 and a substate made of various materials such as quartz- however fails to specify as recited by claims 35 and 36 wherein, the insulating substrate is a high strain point glass including an alkaline-earth alumino-borosilicate glass.

Okabe teaches forming a alkaline-earth alumino-borosilicate glass substrate and an alignment mark formed and detected through visible light (Col.l6, lines: 65-68).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Yudasaka's teachings to further include a alkaline-earth alumino-borosilicate glass substrate and an alignment mark formed and detected through visible light as taught by Okabe because as Okabe teaches, such materials/methods are useful in MOS and BJT applications (Col.6, lines: 65-68).

Allowable Subject Matter

Claim 22 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

In reference to claim 22, prior art fails to teach nor suggest the combination of the limitations of claim 18, wherein, a metal pattern of the MOS single-crystal silicon thin-film transistor is formed under a wiring rule which is more relaxed than a wiring rule of a gate pattern of the MOS single-crystal silicon thin-film transistor.

Claims 28 and 37 are allowed.

Response to Arguments

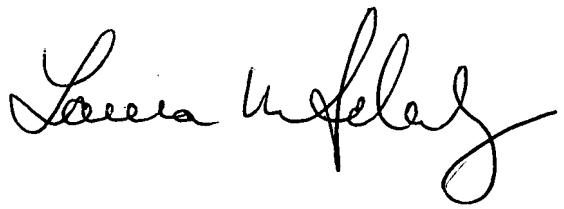
Applicant's arguments filed 5/8/06 have been fully considered but they are not persuasive. Applicant argues that Yudasaka fails to teach the newly added limitations of claim 16- however the language of claim 16 is describing layers with different thicknesses which is disclosed by Yudasaka.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Laura M. Schillinger whose telephone number is (571) 272-1697. The examiner can normally be reached on M-T, R-F 7:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Laura M Schillinger
Primary Examiner
Art Unit 2813

9/27/06